AMENDMENTS TO THE SPECIFICATION

Please amend the specification at Page 4, Line 15 to Page 5, Line 12 as follows:

-- FIG. 1 schematically depicts the layout of the device 100 architecture. Single wall nanotubes (SWNTs) 110 electrically coupled to titanium contacts 102, 104, together with the silicon back gate 106, form the elements of the NTFET architecture. As described herein, nanotube 110 may be immersed in a liquid 108 for sensing of dissolved analytes. NTFETs were fabricated using nanotubes grown by chemical vapor deposition. Iron nanoparticles encased in mesoporous material were spin-coated and patterned on silicon substrates 106 with 200 nm films 107 of thermal SiO2. Nanotubes of 1.5-3.0 nm diameter and 5-10 μm length were grown over the course of 15 minutes of methane flow at 900°C. Hydrogen was added to the gas stream to prevent the deposition of amorphous carbon contaminants. For the devices fabricated, multiple nanotubes connect the source and drain electrodes 102, 104, with electrical characteristics of individual tubes 110 varying from metallic to semiconducting. FIG. 2 shows an atomic force microscopic image of the device 200 with a number of nanotubes 210 crossing the source and drain electrodes 202, 204.

The performance of devices such as these was determined by monitoring the change in the source-drain current Isd as a function of the gate voltage (Vg) while both increasing and decreasing gate voltages; in order to delineate the full Isd(Vg) characteristic. While in devices incorporating a multitude of nanotubes, both metallic and semiconducting nanotubes contribute to the source-drain current, data presented here are derived from devices with only semiconducting nanotubes, for which an off-

state (positive Vg values) the conductivity is close to zero. Device testing procedures were as follows. For measurements in air, pin probes were simply exposed to air. For measurements in conducting liquids, the silicon chips 106 with NTFET devices 100 were glued to aluminum plates 112 and surrounded with epoxy walls defining sample exposure portion 114 to keep the solution on the chip without contacting the gate (to prevent the shorting of the source-drain current to the gate 106). A glass pipette was used to position a drop of test liquid 108 on the chip. --